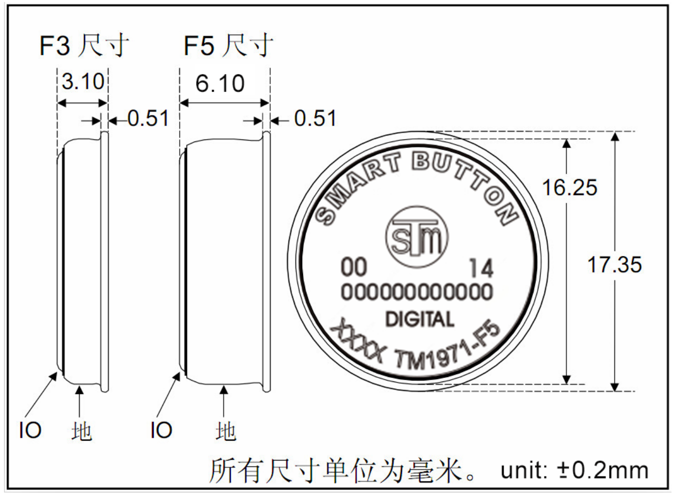
# STM1971
# 256-Bit 1-Wire EEPROM

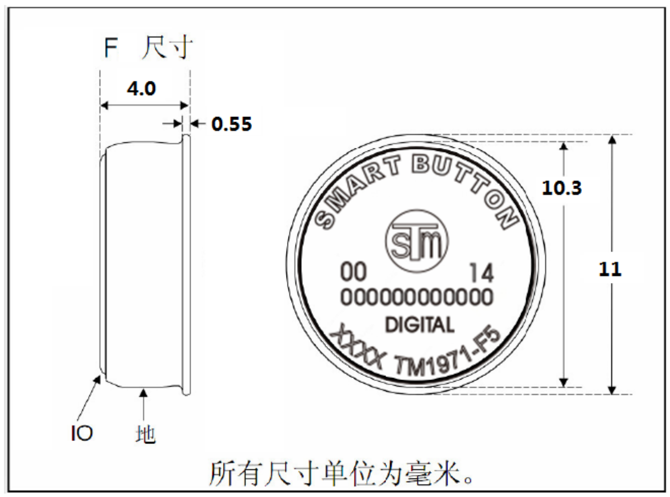
## FEATURES

Read Only Memory (EEPROM) plus 64-bit one-time programmable application register

- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute identity because no two parts are alike
- Built-in multidrop controller ensures compatibility with other MicroLAN products
- EEPROM organized as one page of 32 bytes for random access
- Reduces control, address, data, and power to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 15.3kbits per second
- 8-bit family code specifies STM1971 communication requirements to reader
- Presence detector acknowledges when reader first applies voltage
- Reads and writes over a wide voltage range of 2.8V to 5.25V from -40°C to +85°C

## TM1971 F3 / F4 AND F5 MicroCAN



## DESCRIPTION

The STM1971 256-bit 1-Wire® EEPROM identifies and stores relevant information about the product to which it is associated. This lot or product specific information can be accessed with minimal interface, for example a single port pin of a microcontroller. The STM1971 consists of a factory-lasered registration number that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (14h) plus 256 bits of user-programmable EEPROM and a 64-bit one-time programmable application register. The power to read and write the STM1971 is derived entirely from the 1-Wire communication line. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground return. The 48-bit serial number that is factory-lasered into each STM1971 provides a guaranteed unique identity that allows for absolute traceability. STM1971 to be used easily by human operators. Accessories permit the STM1971 iButton to be mounted on almost any object, including containers, pallets, and bags

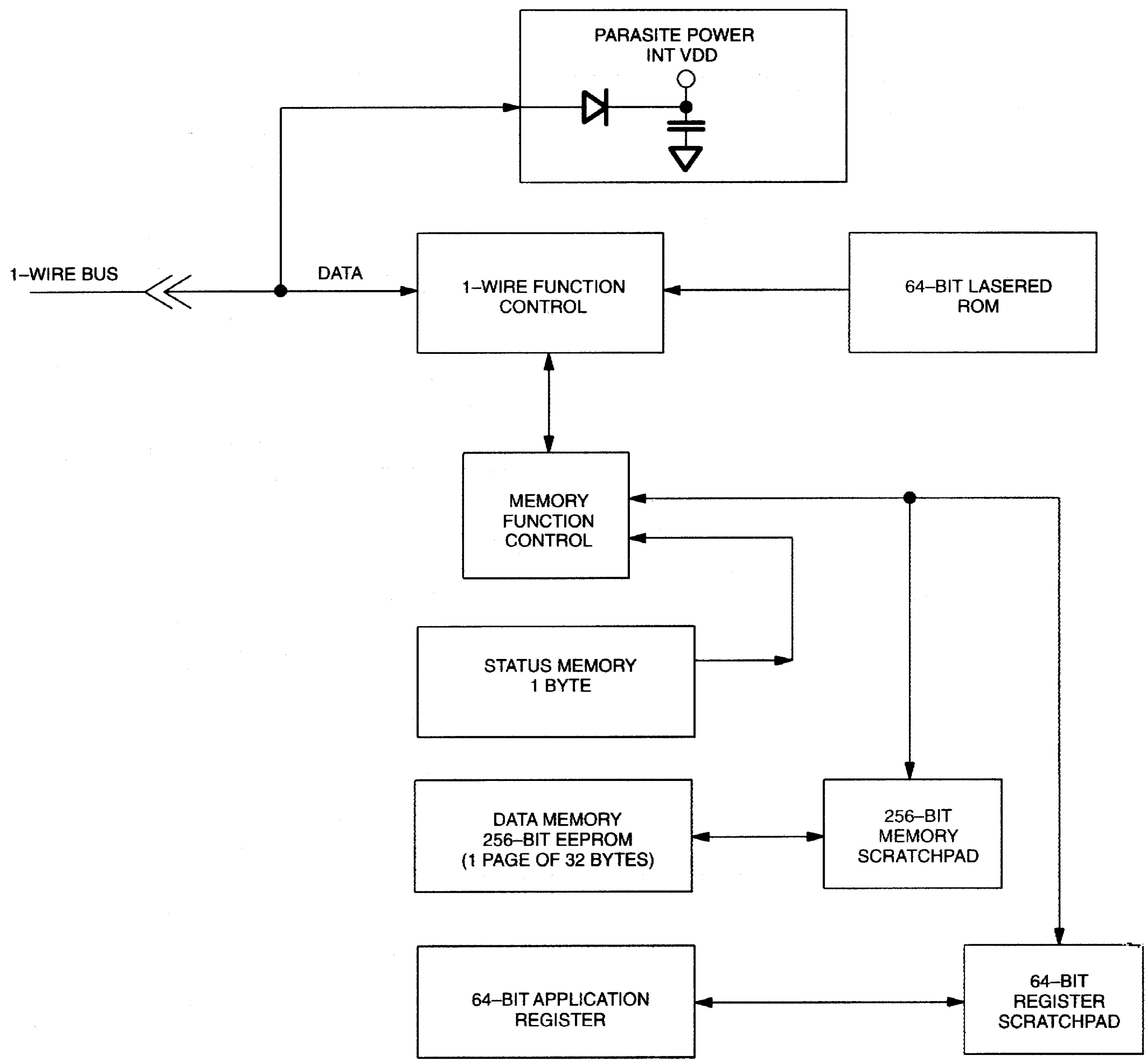
## OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the STM1971. The STM1971 has four main data components: 1) 64-bit lasered ROM, 2) 256-bit EEPROM data memory with scratchpad, 3) 64-bit one-time programmable application register with scratchpad and 4) 8-bit status memory. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the four ROM Function Commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM. The protocol required for these ROM Function Commands is described in Figure 8. After a ROM Function Command is successfully executed, the memory functions become accessible and the master can provide any one of the four memory function commands. The protocol for these memory function commands is described in Figure 6. All data is read and written least significant bit first.

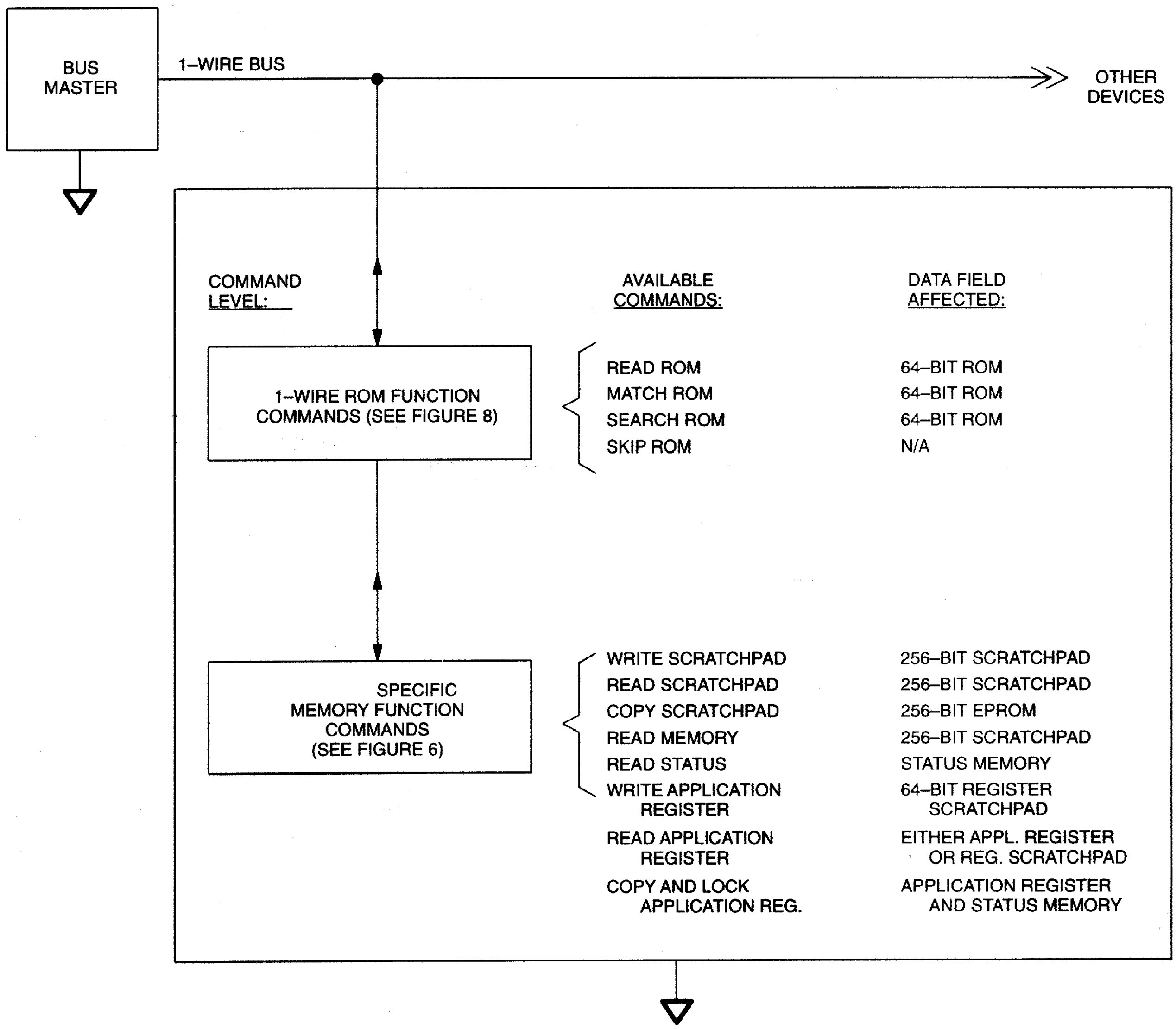
## 64-BIT LASERED ROM

Each STM1971 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family Code (14). The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. (Figure 3). The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire CRC is available in *Application Note 27*. The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the $8^{th}$ bit of the family code has been entered, then the serial number is entered. After the $48^{th}$ bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all 0s.

## **STM1971 BLOCK DIAGRAM** Figure 1



## **HIERARCHICAL STRUCTURE FOR 1-WIRE PROTOCOL** Figure 2

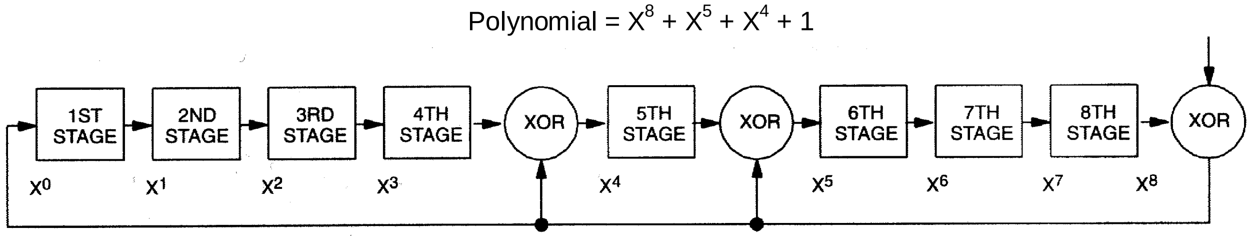



## **64-BIT LASERED ROM** Figure 3

| 8-Bit CRC Code | | 48-Bit Serial Number | | 8-Bit Family Code (14H) | |
|---|---|---|---|---|---|
| MSB | LSB | MSB | LSB | MSB | LSB |

## **1-WIRE CRC GENERATOR** Figure 4

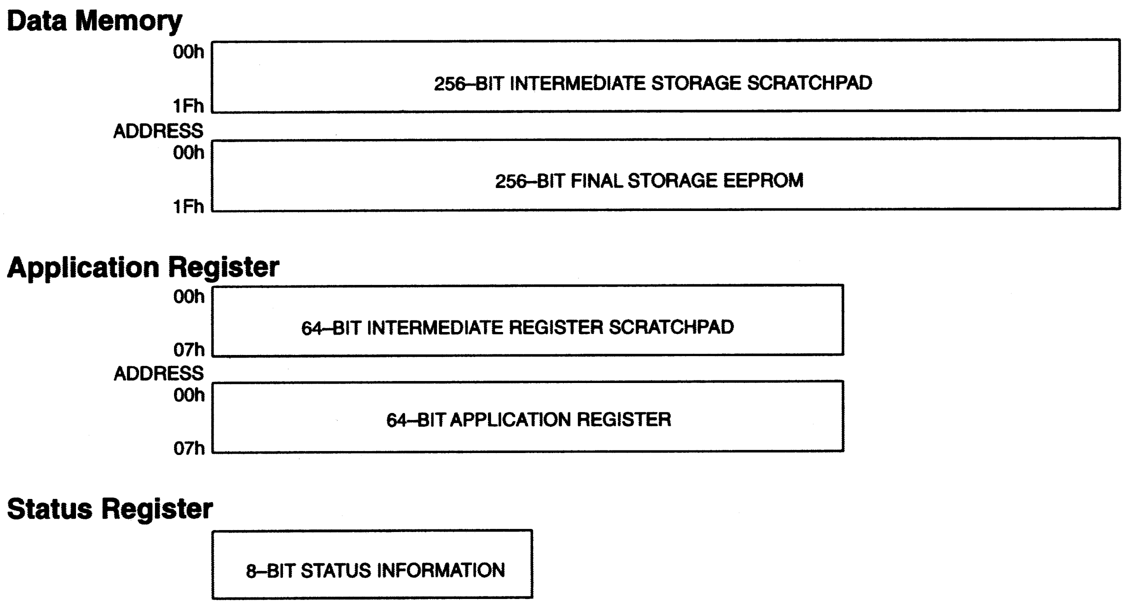
Polynomial = $X^8 + X^5 + X^4 + 1$



## MEMORY

The memory of the STM1971 consists of three separate sections, called data memory, application register, and status register (Figure 5). The data memory and the application register each have its own intermediate storage area called scratchpad that acts as a buffer when writing to the device. The data memory can be read and written as often as desired. The application register, however, is one-time programmable only. Once the application register is programmed, it is automatically write protected. The status register indicates whether the application register is already locked or whether it is still available for storing data. As long as the application register is unprogrammed, the status register reads FFh. Copying data from the register scratchpad to the application register clears the 2 least significant bits of the status register, yielding an FCh the next time one reads the status register.

## STM1971 MEMORY MAP Figure 5




## MEMORY FUNCTION COMMANDS

The Memory Function Flow Chart (Figure 6) describes the protocols necessary for accessing the different memory sections of the STM1971. An example is shown later in this document.

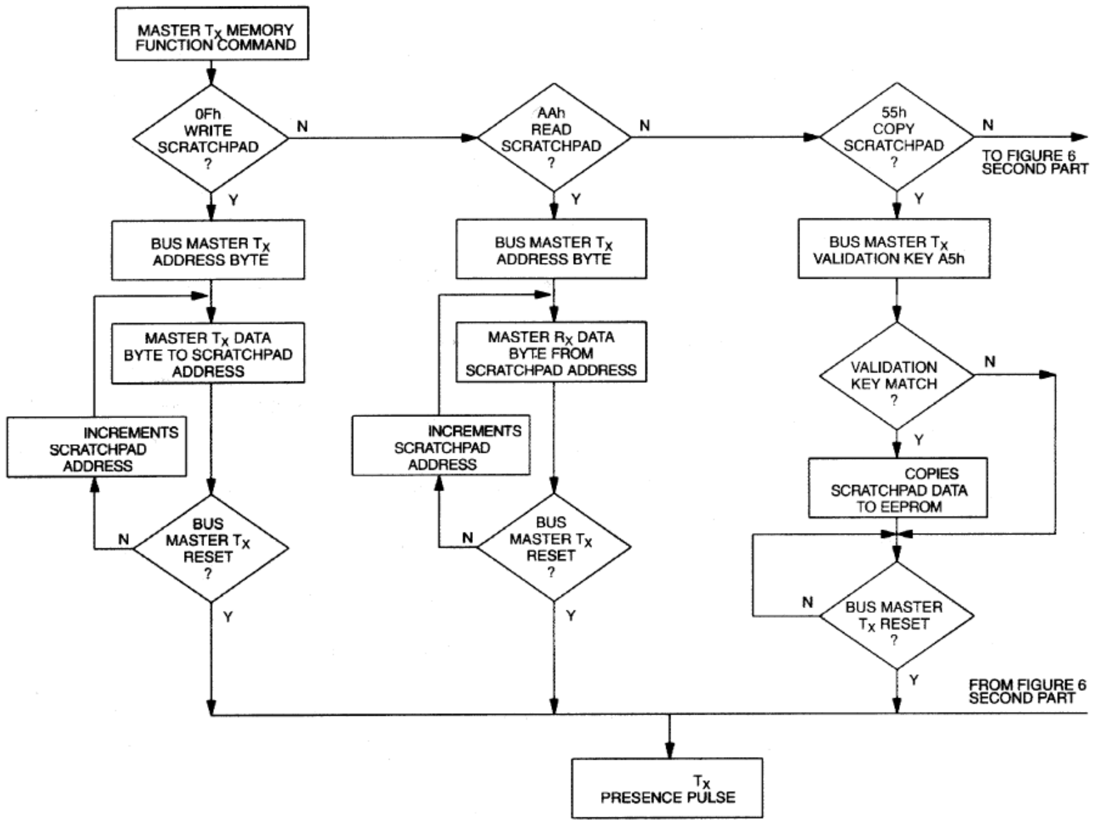
## WRITE SCRATCHPAD [0Fh]

After issuing the Write Scratchpad command, the master must first provide a 1-byte address, followed by the data to be written to the scratchpad for the data memory. The STM1971 automatically increments the address after every byte it receives. After having received a data byte for address 1Fh, the address counter wraps around to 00h for the next byte and writing continues until the master sends a Reset Pulse.

## READ SCRATCHPAD [AAh]

This command is used to verify data previously written to the scratchpad before it is copied into the final storage EEPROM memory. After issuing the Read Scratchpad command, the master must provide the 1-byte starting address from where data is to be read. The STM1971 automatically increments the address after every byte read by the master. After the data at address 1Fh has been read, the address counter wraps around to 00h for the next byte and reading continues until the master sends a Reset Pulse.

## MEMORY FUNCTION FLOW CHART Figure 6



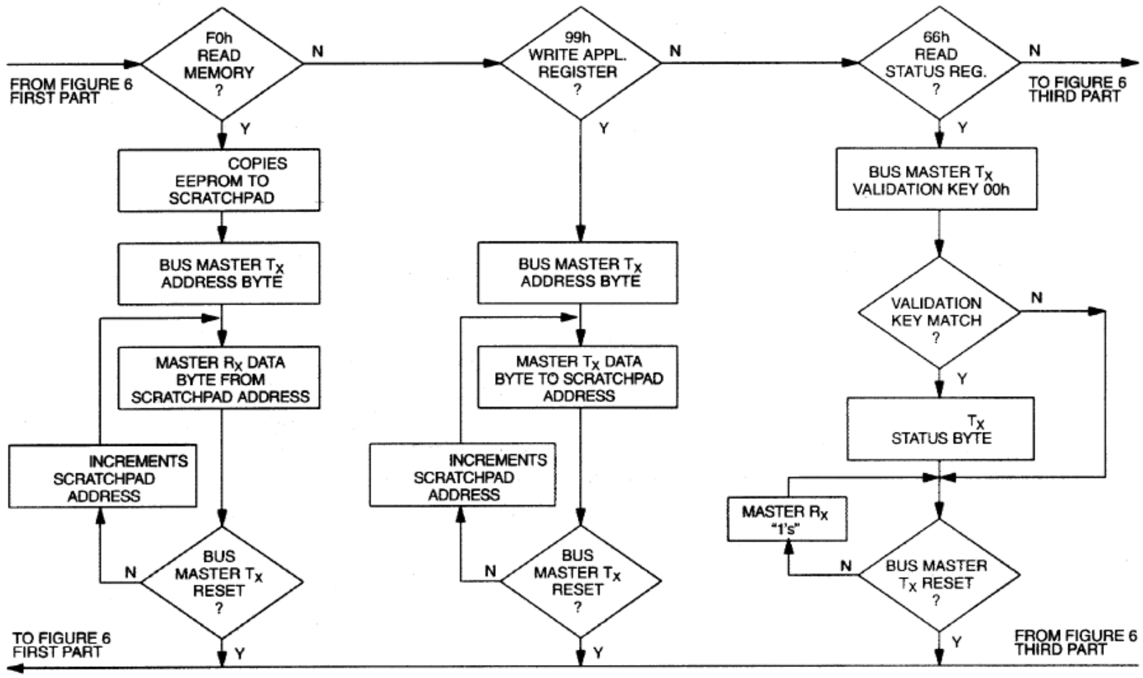

## COPY SCRATCHPAD [55h]

After the data stored in the scratchpad has been verified the master may send the Copy Scratchpad command followed by a validation key of A5h to transfer data from the scratchpad to the EEPROM memory. This command always copies the data of the entire scratchpad. Therefore, if one desires to change only a few bytes of the EEPROM data, the scratchpad should contain a copy of the latest EEPROM data before the Write Scratchpad and Copy Scratchpad commands are issued. After this command and the validation key are issued, the data line must be held above $V_{PUPmin}$ for at least $t_{PROG}$.

## READ MEMORY [F0h]

The Read Memory command is used to read a portion or all of the EEPROM data memory and to copy the entire data memory into the scratchpad to prepare for changing a few bytes. To copy data from the data memory to the scratchpad and to read it, the master must issue the read memory command followed by the 1-byte starting address of the data to be read from the scratchpad. The STM1971 automatically increments the address after every byte read by the master. After the data of address 1Fh has been read, the address counter wraps around to 00h for the next byte and reading continues until the master sends a Reset Pulse. If one intends to copy the entire data memory to the scratchpad without reading data, a starting address is not required; the master may send a Reset Pulse immediately following the command code.

## **MEMORY FUNCTION FLOW CHART** Figure 6 (continued)



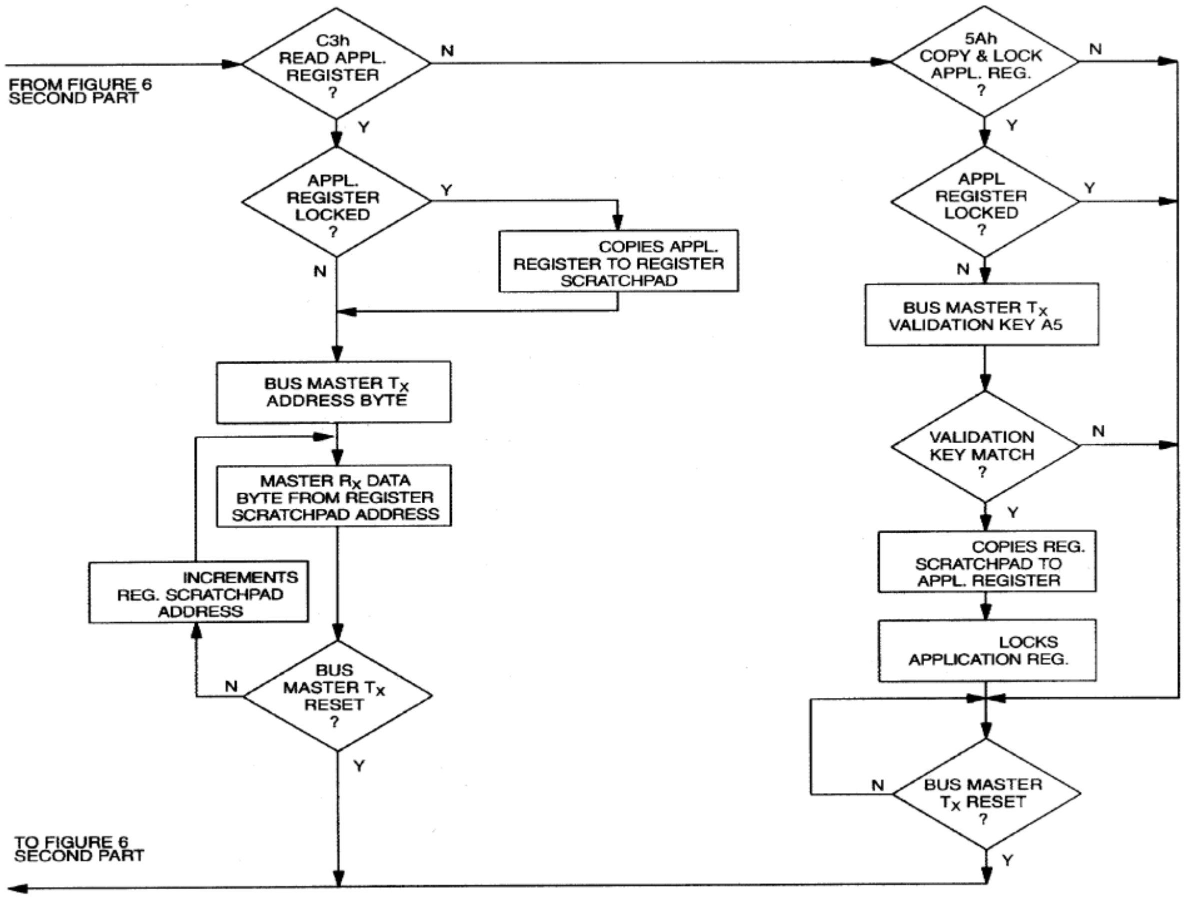

## WRITE APPLICATION REGISTER [99h]

This command is essentially the same as the Write Scratchpad command, but it addresses the 64-bit register scratchpad. After issuing the command code, the master must provide a 1-byte address, followed by the data to be written. The STM1971 automatically increments the address after every byte it receives. After receiving the data byte for address 07h, the address counter wraps around to 00h for the next byte and writing continues until the master sends a Reset Pulse. The Write Application Register command can be used as long as the application register has not yet been locked. If issued for a device with the application register locked, the data written to the register scratchpad will be lost.

## READ STATUS REGISTER [66h]

The status register is a means for the master to find out whether the application register has been programmed and locked. After issuing the read status register command, the master must provide the validation key 00h before receiving status information. The two least significant bits of the 8-bit status register are 0 if the application register was programmed and locked; all other bits always read 1. The master may finish the read status command by sending a Reset Pulse at any time.

## MEMORY FUNCTION FLOW CHART Figure 6 (continued)




## READ APPLICATION REGISTER [C3h]

This command is used to read the application register or the register scratchpad. As long as the application register is not yet locked, the STM1971 transmits data from the register scratchpad. After the application register is locked the STM1971 transmits data from the application register, making the register scratchpad inaccessible for reading. The contents of the status register indicate where the data received with this command came from. After issuing the Read Application Register command, the master must provide the 1-byte starting address from where data is to be read. The STM1971 automatically increments the address after every byte read by the master. After the data at address 07h has been read, the address counter wraps around to 00h for the next byte and reading continues until the master sends a Reset Pulse.

## COPY & LOCK APPLICATION REGISTER [5Ah]

After the data stored in the register scratchpad has been verified the master may send the Copy & Lock Application Register command followed by a validation key of A5h to transfer the contents of the entire register scratchpad to the application register and to simultaneously write-protect it. The master may cancel this command by sending a Reset Pulse instead of the validation key. After the validation key is transmitted, the data line must be held above $V_{PUPmin}$ for at least $t_{PROG}$. Once $t_{PROG}$ has expired, the application register will contain the data of the register scratchpad. Further write accesses to the application register will be denied. **The Copy & Lock Application Register command can only be executed once.**

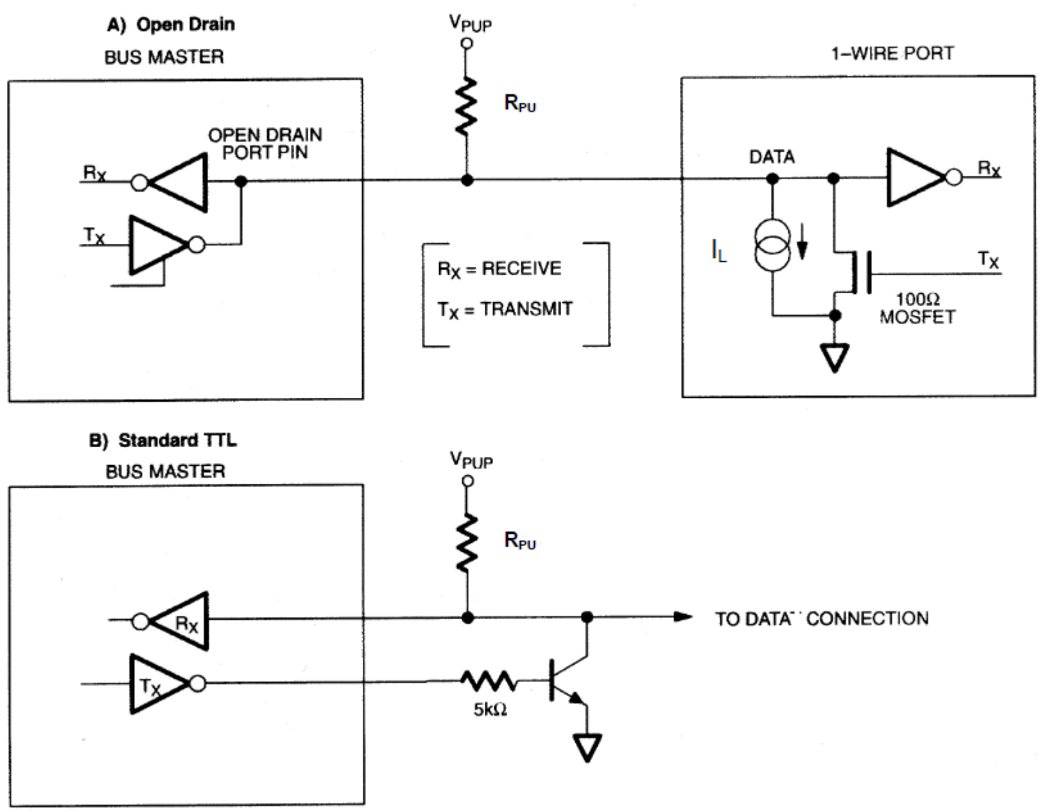
# 1-WIRE BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances, the STM1971 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal type and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master.

## Hardware Configuration

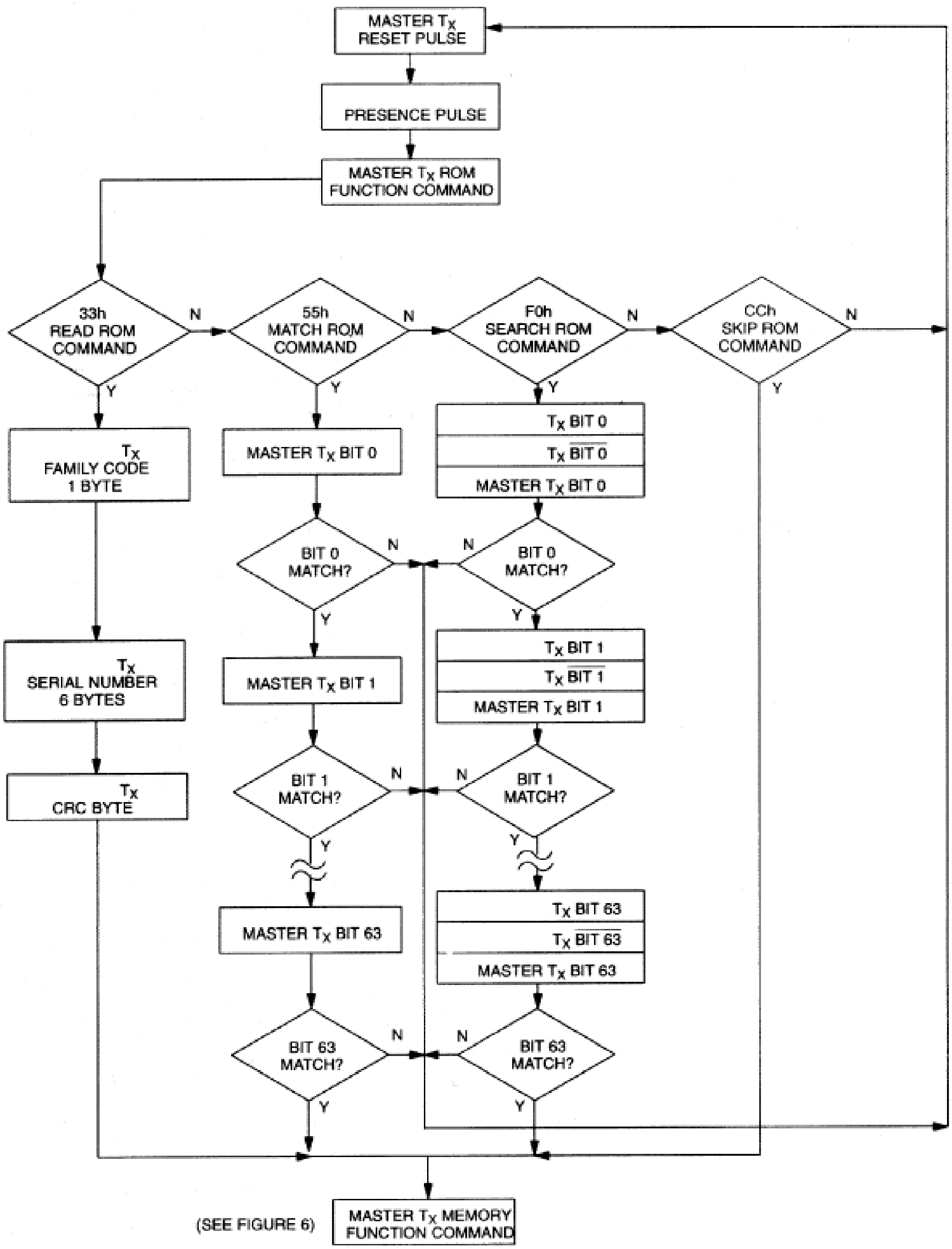
The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain connection or three-state outputs. The 1-Wire port of the STM1971 is open drain with an internal circuit equivalent to that shown in Figure 7. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The STM1971 communicates at regular 1-Wire speed, 15.3kbits per second, and requires a pullup resistor as shown in Figure 7. The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120µs, one or more of the devices on the bus may be reset.

## **HARDWARE CONFIGURATION** Figure 7




Note: Depending on the 1-Wire communication speed and the bus characteristics, the optimal pullup resistor value will be in the 0.3k& to 2.2k& range. To write to a single device, a $R_{PUPmax}$ resistor and $V_{PUP}$ of at least 4.0V is sufficient. For writing multiple STM1971s simultaneously or operation at low $V_{PUP}$, the resistor should be bypassed by a low-impedance pullup to $V_{PUP}$ while the device copies the scratchpad to EEPROM.

## **ROM FUNCTIONS FLOW CHART** Figure 8



## Transaction Sequence

The sequence for accessing the STM1971 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

## INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a Reset Pulse transmitted by the bus master followed by a Presence Pulse(s) transmitted by the slave(s).

The Presence Pulse lets the bus master know that the STM1971 is on the bus and is ready to operate. For more details, see the 1-Wire Signaling section.

## ROM FUNCTION COMMANDS

Once the bus master has detected a presence pulse, it can issue one of the four ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 8):

### Read ROM [33h]

This command allows the bus master to read the STM1971's 8-bit family code, 48-bit serial number, and 8-bit CRC. This command can be used only if there is a single STM1971 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number usually result in a mismatch of the CRC.

### Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific STM1971 on a multidrop bus. Only the STM1971 that exactly matches the 64-bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a Reset Pulse. This command can be used with a single or multiple devices on the bus.

### Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns produces a wired-AND result).

### Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The Search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The Search ROM process is the repetition of a simple, three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, three-step routine on each bit of the ROM.

After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See *Application Note 187* for a comprehensive discussion of a search ROM, including an actual example.

## 1-Wire Signaling

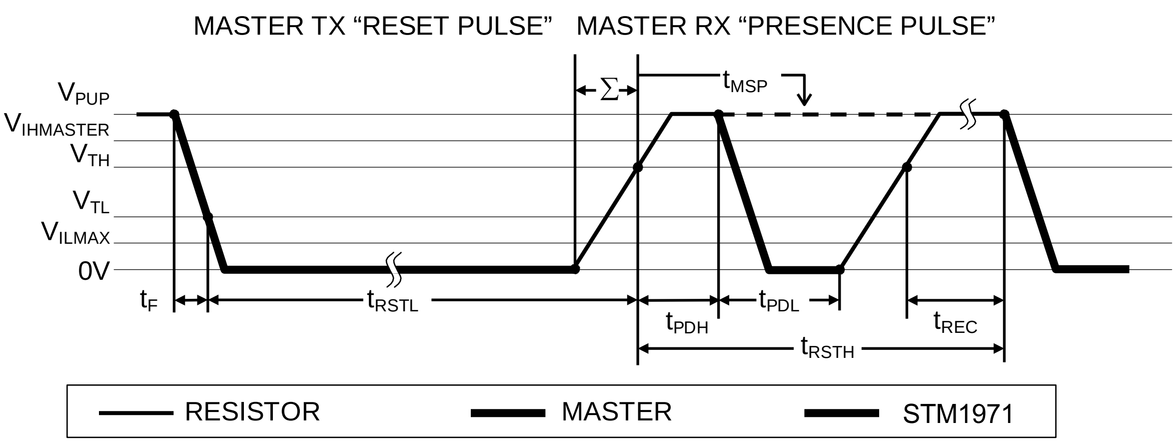
The STM1971 requires strict protocols to insure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write-0, Write-1 and Read- Data. All these signals (except Presence Pulse) are initiated by the bus master.

To get from idle to active, the voltage on the 1-Wire line needs to fall from $V_{PUP}$ below the threshold $V_{TL}$. To get from active to idle, the voltage needs to rise from $V_{ILMAX}$ past the threshold $V_{TH}$. The time it takes for the voltage to make this rise is seen in Figure 9 as $\sum$, and its duration depends on the pullup resistor ($R_{PUP}$) used and the capacitance of the 1-Wire network attached. The voltage $V_{ILMAX}$ is relevant for the STM1971 when determining a logical level, not triggering any events.

Figure 9 shows the initialization sequence required to begin any communication with the STM1971. A Reset Pulse followed by a Presence Pulse indicates the STM1971 is ready to receive data, given the correct ROM and memory function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge.

After the bus master has released the line it goes into Receive mode. Now the 1-Wire bus is pulled to $V_{PUP}$ through the pullup resistor. When the threshold $V_{TH}$ is crossed, the STM1971 waits for $t_{PDH}$ and then transmits a Presence Pulse by pulling the line low for $t_{PDL}$. To detect a Presence Pulse, the master must test the logical state of the 1-Wire line at $t_{MSP}$. The $t_{RSTH}$ window must be at least the sum of $t_{PDHMAX}$, $t_{PDLMAX}$, and $t_{RECMIN}$. Immediately after $t_{RSTH}$ is expired, the STM1971 is ready for data communication.

## INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 9




## Read/Write Time Slots

Data communication with the STM1971 takes place in time slots, which carry a single bit each. Write time slots transport data from bus master to slave. Read time slots transfer data from slave to master. Figure 10 illustrates the definitions of the write and read time slots.

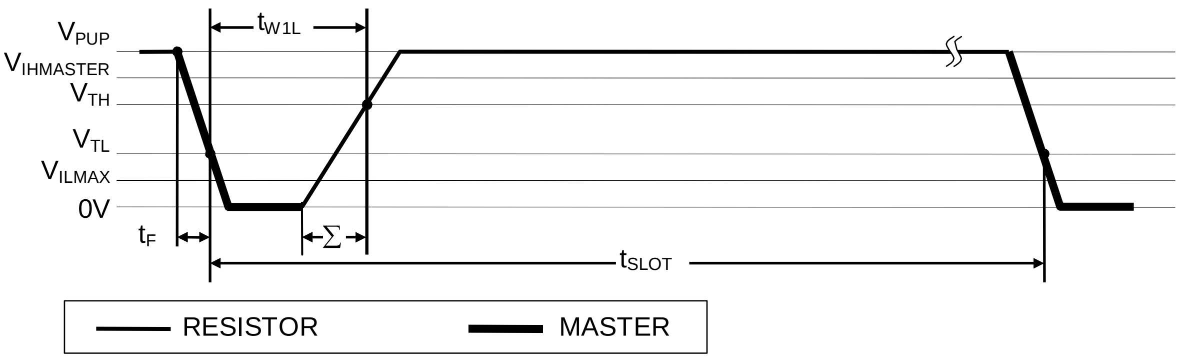
All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold $V_{TL}$, the STM1971 starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

## Master-to-Slave

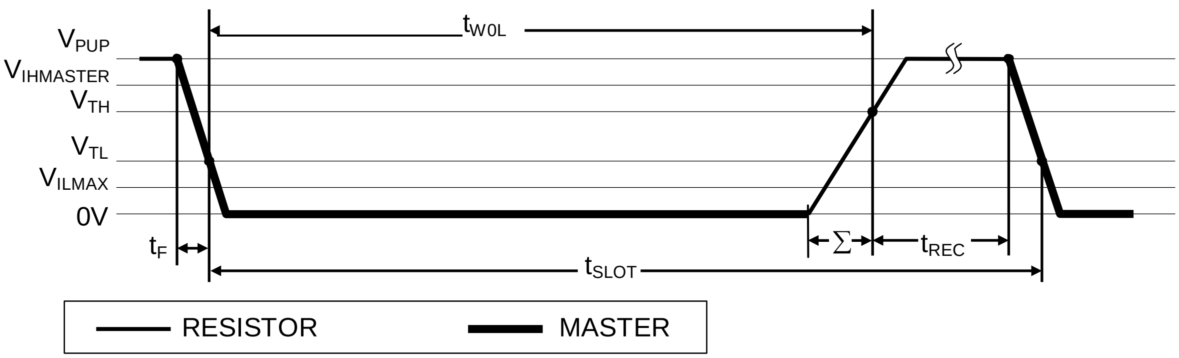
For a **Write-1** time slot, the voltage on the data line must have crossed the $V_{TH}$ threshold before the Write-1 low time $t_{W1LMAX}$ is expired. For a **Write-0** time slot, the voltage on the data line must stay below the $V_{TH}$ threshold until the Write-0 low time $t_{W0LMIN}$ is expired. For the most reliable communication, the voltage on the data line should not exceed $V_{ILMAX}$ during the entire $t_{W0L}$ or $t_{W1L}$ window. After the $V_{TH}$ threshold has been crossed, the STM1971 needs a recovery time $t_{REC}$ before it is ready for the next time slot.

## **READ/WRITE TIMING DIAGRAM** Figure 10

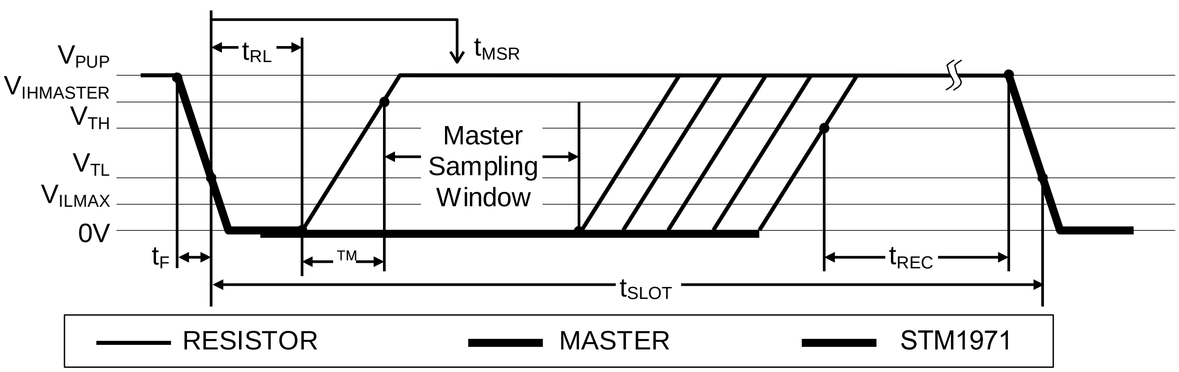
### Write-1 Time Slot




### Write-0 Time Slot




### Read-data Time Slot



## Slave-to-Master

A **Read-data** time slot begins like a Write-1 time slot. The voltage on the data line must remain below $V_{TL}$ until the read low time $t_{RL}$ is expired. During the $t_{RL}$ window, when responding with a 0, the STM1971 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the STM1971 does not hold the data line low at all, and the voltage starts rising as soon as $t_{RL}$ is over.

The sum of $t_{RL}$ + ™ (rise time) on one side and the internal timing generator of the STM1971 on the other side define the master sampling window ($t_{MSRMIN}$ to $t_{MSRMAX}$) in which the master must perform a read from the data line. For the most reliable communication, $t_{RL}$ should be as short as permissible, and the master should read close to but no later than $t_{MSRMAX}$. After reading from the data line, the master must wait until $t_{SLOT}$ is expired. This guarantees sufficient recovery time $t_{REC}$ for the STM1971 to get ready for the next time slot. Note that $t_{REC}$ specified herein applies only to a single STM1971 attached to a 1-Wire line. For multidevice configurations, $t_{REC}$ must be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the DS2482-x00 or DS2480B 1-Wire line drivers can be used.

## IMPROVED NETWORK BEHAVIOR (SWITCHPOINT HYSTERESIS)

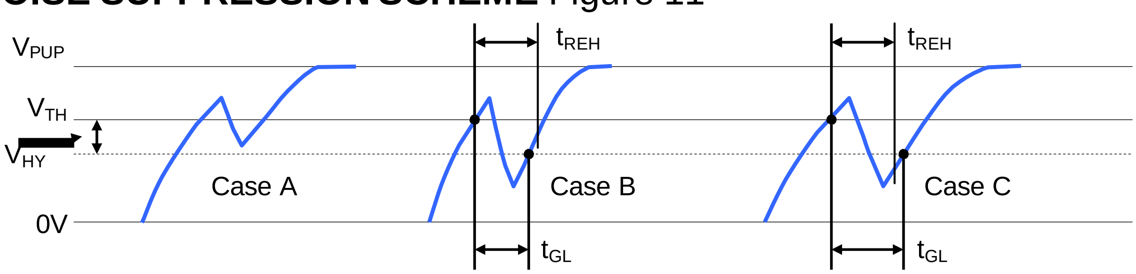
In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up, or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the STM1971 uses a new 1-Wire front end, which makes it less sensitive to noise.

The 1-Wire front end of the STM1971 differs from traditional slave devices in three characteristics.

1) There is additional low-pass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise.
2) There is a hysteresis at the low-to-high switching threshold $V_{TH}$. If a negative glitch crosses $V_{TH}$ but does not go below $V_{TH}$ - $V_{HY}$, it will not be recognized (Figure 11, Case A)..
3) There is a time window specified by the rising edge hold-off time $t_{REH}$ during which glitches are ignored, even if they extend below $V_{TH}$ - $V_{HY}$ threshold (Figure 11, Case B, $t_{GL} < t_{REH}$). Deep voltage droops or glitches that appear late after crossing the $V_{TH}$ threshold and extend beyond the $t_{REH}$ window cannot be filtered out and are taken as the beginning of a new time slot (Figure 11, Case C, $t_{GL}$ ε $t_{REH}$).

Devices that have the parameters $V_{HY}$, and $t_{REH}$ specified in their electrical characteristics use the improved 1-Wire front end.

## NOISE SUPPRESSION SCHEME Figure 11



# MEMORY FUNCTION EXAMPLE

Example: Write 2 data bytes to data memory locations 0006h and 0007h. Read entire data memory.

| MASTER MODE | DATA (LSB FIRST) | COMMENTS |
|---|---|---|
| TX | Reset | Reset pulse (480µs to 960µs) |
| RX | Presence | Presence pulse |
| TX | CCh | Issue "Skip ROM" command |
| TX | 0Fh | Issue "Write Scratchpad" command |
| TX | 06h | Start address = 06h |
| TX | <2 Data Bytes> | Write 2 bytes of data to scratchpad |
| TX | Reset | Reset pulse |
| RX | Presence | Presence pulse |
| TX | CCh | Issue "Skip ROM" command |
| TX | AAh | Issue "Read Scratchpad" command |
| TX | 06h | Start address = 06h |
| RX | <2 Data Bytes> | Read scratchpad data and verify |
| TX | Reset | Reset pulse |
| RX | Presence | Presence pulse |
| TX | CCh | Issue "Skip ROM" command |
| TX | 55h | Issue "Copy Scratchpad" command |
| TX | A5h | Validation key |
| TX | <Data Line High> | Data line must be above $V_{PUPmin}$ for $t_{PROG}$. |
| TX | Reset | Reset pulse |
| RX | Presence | Presence pulse |
| TX | CCh | Issue "Skip ROM" command |
| TX | F0h | Issue "Read Memory" command |
| TX | 00h | Start address = 00h |
| RX | <32 Bytes> | Read EEPROM data page |
| TX | Reset | Reset pulse |
| RX | Presence | Presence pulse |

# ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Voltage Range on DATA to Ground | -0.5V to +6.0V |
| DATA Sink Current | 20mA |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -55°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Soldering Temperature (reflow) | |

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.*

# ELECTRICAL CHARACTERISTICS

($T_A$ = -40°C to +85°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DATA PIN GENERAL DATA** | | | | | | |
| 1-Wire Pullup Voltage | $V_{PUP}$ | (Notes 2) | 2.8 | | 5.25 | V |
| 1-Wire Pullup Resistance | $R_{PUP}$ | (Notes 2, 3) | 0.3 | | 2.2 | k& |
| Input Capacitance | $C_{IO}$ | (Notes 4, 5) | | | 1000 | pF |
| Input Load Current | $I_L$ | DATA pin at $V_{PUP}$ | 0.05 | | 15 | µA |
| High-to-Low Switching Threshold | $V_{TL}$ | (Notes 5, 6, 7) | 0.46 | | $V_{PUP}$ - 1.8V | V |
| Input Low Voltage | $V_{IL}$ | (Notes 2, 8) | | | 0.5 | V |
| Low-to-High Switching Threshold | $V_{TH}$ | (Notes 5, 6, 9) | 1.0 | | $V_{PUP}$ - 1.1V | V |
| Switching Hysteresis | $V_{HY}$ | (Notes 5, 6, 10) | 0.21 | | 1.70 | V |
| Output Low Voltage | $V_{OL}$ | At 4mA (Note 11) | | | 0.4 | V |
| Recovery Time | $t_{REC}$ | $R_{PUP}$ = 2.2k& (Notes 2,12) | 5 | | | µs |
| Rising-Edge Hold-off Time | $t_{REH}$ | (Notes 5, 13) | 0.5 | | 5.0 | µs |
| Timeslot Duration | $t_{SLOT}$ | (Notes 2, 14) | 65 | | | µs |
| **DATA PIN, 1-WIRE RESET, PRESENCE DETECT CYCLE** | | | | | | |
| Reset Low Time | $t_{RSTL}$ | (Note 2) | 480 | | 960 | µs |
| Presence Detect High Time | $t_{PDH}$ | | 15 | | 60 | µs |
| Presence Detect Low Time | $t_{PDL}$ | | 60 | | 240 | µs |
| Presence Detect Sample Time | $t_{MSP}$ | (Notes 2, 15) | 60 | | 75 | µs |
| **DATA PIN, 1-Wire WRITE** | | | | | | |
| Write-0 Low Time | $t_{W0L}$ | (Notes 2, 16) | 60 | | 120 - ∑ | µs |
| Write-1 Low Time | $t_{W1L}$ | (Notes 2, 16) | 1 | | 15 - ∑ | µs |
| **DATA PIN, 1-Wire READ** | | | | | | |
| Read Low Time | $t_{RL}$ | (Notes 2, 17) | 1 | | 15 - ™ | µs |
| Read Sample Time | $t_{MSR}$ | (Notes 2, 17) | $t_{RL}$ + ™ | | 15 | µs |
| **EEPROM** | | | | | | |
| Programming Current | $I_{PROG}$ | (Notes 5, 18) | | | 0.5 | mA |
| Programming Time | $t_{PROG}$ | (Note 19) | | | 10 | ms |
| Write/Erase Cycles (Endurance) (Notes 20, 21) | $N_{CY}$ | | 1k | | | \| |
| Data Retention (Notes 22, 23, 24) | $t_{DR}$ | At 85°C (worst case) | 40 | | | years |

# ELECTRICAL CHARACTERISTICS (continued)

($T_A$ = -40°C to +85°C, unless otherwise noted.) (Note 1)

**Note 1:** Limits are 100% production tested at $T_A$ = +25°C and/or $T_A$ = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.

**Note 2:** System requirement.

**Note 3:** Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum $t_{REC}$. For more heavily loaded systems, an active pullup such as that found in the DS2482-x00, DS2480B, or DS2490 may be required. If longer $t_{REC}$ is used, higher $R_{PUP}$ values may be able to be tolerated.

**Note 4:** Maximum value represents the internal parasite capacitance when $V_{PUP}$ is first applied. If a 2.2k& resistor is used to pull up the data line, 2.5µs after $V_{PUP}$ has been applied the parasite capacitance will not affect normal communications.

**Note 5:** Guaranteed by design, characterization and/or simulation only. Not production tested.

**Note 6:** $V_{TL}$, $V_{TH}$, and $V_{HY}$ are a function of the internal supply voltage which is itself a function of $V_{PUP}$, $R_{PUP}$, 1-Wire timing, and capacitive loading on DATA. Lower $V_{PUP}$, higher $R_{PUP}$, shorter $t_{REC}$, and heavier capacitive loading all lead to lower values of $V_{TL}$, $V_{TH}$, and $V_{HY}$.

**Note 7:** Voltage below which, during a falling edge on DATA, a logic 0 is detected.

**Note 8:** The voltage on DATA needs to be less or equal to $V_{IL(MAX)}$ at all times the master is driving DATA to a logic-0 level.

**Note 9:** Voltage above which, during a rising edge on DATA, a logic 1 is detected.

**Note 10:** After $V_{TH}$ is crossed during a rising edge on DATA, the voltage on DATA has to drop by at least $V_{HY}$ to be detected as logic '0'.

**Note 11:** The I-V characteristic is linear for voltages less than 1V.

**Note 12:** Applies to a single device attached to a 1-Wire line.

**Note 13:** The earliest recognition of a negative edge is possible at $t_{REH}$ after $V_{TH}$ has been reached on the preceding rising edge.

**Note 14:** Defines maximum possible bit rate. Equal to $1/(t_{W0L(min)} + t_{REC(min)})$.

**Note 15:** Interval after $t_{RSTL}$ during which a bus master is guaranteed to sample a logic-0 on DATA if there is a
STM7100 present. Minimum limit is $t_{PDH(max)}$; maximum limit is $t_{PDH(min)} + t_{PDL(min)}$.

**Note 16:** ∑ in Figure 10 represents the time required for the pullup circuitry to pull the voltage on DATA up from $V_{IL}$ to $V_{TH}$. The actual maximum duration for the master to pull the line low is $t_{W1Lmax} + t_F$ and $t_{W0Lmax} + t_F$ respectively.

**Note 17:** ™ in Figure 10 represents the time required for the pullup circuitry to pull the voltage on DATA up from $V_{IL}$ to the input high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLmax} + t_F$.

**Note 18:** Current drawn from DATA during the EEPROM programming interval. The pullup circuit on DATA during the programming interval should be such that the voltage at DATA is greater than or equal to $V_{PUPMIN}$. If $V_{PUP}$ in the system is close to $V_{PUPMIN}$, a low-impedance bypass of $R_{PUP}$, which can be activated during programming, may need to be added.

**Note 19:** Interval begins $t_{REHmax}$ after the trailing rising edge on DATA for the last timeslot of the validation key for a valid copy sequence. Interval ends once the device's self-timed EEPROM programming cycle is complete and the current drawn by the device has returned from $I_{PROG}$ to $I_L$.

**Note 20:** Write-cycle endurance is degraded as $T_A$ increases.

**Note 21:** Not 100% production-tested; guaranteed by reliability monitor sampling.

**Note 22:** Data retention is degraded as $T_A$ increases.

**Note 23:** Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to data sheet limit at operating temperature range is established by reliability testing.

**Note 24:** EEPROM writes can become nonfunctional after the data-retention time is exceeded. Long-term storage at elevated temperatures is not recommended; the device can lose its write capability after 10 years at +125°C or 40 years at +85°C.